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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,327	01/17/2002	Fong-Long Lin	2102397-992080	3924

7590 08/27/2004

David L. Alberti
Gray Cary Ware & Freidenrich
1755 Embarcadero Road
Palo Alto, CA 94303

EXAMINER	
BAKER, PAUL A	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 08/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,327	LIN ET AL.	
	Examiner	Art Unit	
	Paul A Baker	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/23/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement filed 23 October 2003 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because copending case 10/206,635 is not a patent document, copending cases submitted via IDS must be listed under other documents since an application is not a patent until the merits of the application have been considered. It has been placed in the application file, the information referred to therein has been considered as to the merits given applicant's intent with this disclosure is discernable. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 10 recites the limitation "micro-control unit" in line 2. There is insufficient antecedent basis for this limitation in the claim. For the purpose of examination claim 10 will be considered to be dependent upon claim 9.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7, and 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Padgaonkar et al. US Patent 5,014,191.

In regards to claim 1, Padgaonkar discloses a single integrated circuit microcontroller comprising:

an erasable/programmable non-volatile memory unit in figure 2 element 108;

a read protection flag stored within said microcontroller in figure 2 element 202; and

a logic portion which is adapted to detect when a special mode is activated, to check said read protection flag upon detecting a special mode, and to allow external access to said non-volatile memory unit only if said special mode is activated and said read protection flag is cleared in figure 2 element 200 and column 1 line 66 through column 2 line 5.

In regards to claim 2, Padgaonkar discloses said non-volatile memory unit is adapted to store certain firmware, and wherein logic portion is further adapted to alter said certain firmware if said read protection flag is set and said special mode is

activated, and to clear said read protection flag after said firmware is altered in column 2 lines 15-22 and 40-44.

In regards to claim 3, Padgaonkar discloses said logic portion is adapted to erase said certain firmware if said read protection flag is set and said special mode is activated, and to clear said read protection flag after said firmware is erased in column 2 lines 15-22 and 40-44.

In regards to claim 4, Padgaonkar discloses said logic portion is adapted to program over said certain firmware if said read protection flag is set and said special mode is activated, and to clear said read protection flag after said programming is complete in column 2 lines 15-22.

In regards to claim 5, Padgaonkar said logic portion is further adapted to erase said non-volatile memory unit if said read protection flag is set and said special mode is activated, and to allow external access to said non-volatile memory unit after said non-volatile memory unit is erased in column 2 lines 40-44.

In regards to claim 7, Padgaonkar discloses the application of his invention to all non-volatile memories in column 1 lines 39-43, therefore Padgaonkar anticipates said erasable/programmable non-volatile memory unit comprises a flash memory unit.

In regards to claim 20, Padgaonkar discloses a method for providing read protection for a microcontroller including an embedded programmable non-volatile memory unit having a first portion that stores certain firmware, and a special mode in which said programmable non-volatile memory unit is externally accessible, said method comprising the steps of:

storing a read protection flag in said microcontroller in figure 2 element 202;

detecting when said special mode is activated in figure 3 MC/MP input;

checking said read protection flag when said special mode is activated in figure 3 SO input; and

allowing external access to said first portion of said memory unit only if said read protection flag is cleared via figure 3 READ output in conjunction with INT and EXT outputs.

In regards to claim 21, Padgaonkar discloses the invention disclosed in claim 20 and further comprising the steps of:

detecting a request to access said first portion of said memory while said special mode is activated in figure 2 element 208 in conjunction with figure 3 TR and MC/MP input;

erasing said first portion of said memory unit upon detecting said request if said read protection flag is set in column 2 lines 40-44;

clearing said read protection flag after said first portion of said memory unit is erased in column 2 lines 15-22; and

allowing access to said first portion of said memory unit is inherent given column 2 lines 15-22 in view of column 3 lines 33-47 (once the protection bits are erased access to the non-volatile memory (NVM) is restored).

In regards to claim 22, Padgaonkar discloses the invention disclosed in claim 20 and further comprising the steps of:

detecting a request to access said first portion of said memory unit while said special mode is activated in figure 2 element 208 in conjunction with figure 3 TR and MC/MP input;

reprogramming said first portion of said memory unit upon detecting said request if said read protection flag is set in column 2 lines 40-44;

clearing said read protection flag after said first portion of said memory unit is reprogrammed in column 2 lines 15-22; and

allowing access to said first portion of said memory unit is inherent given column 2 lines 15-22 in view of column 3 lines 33-47 (once the protection bits are erased access to the non-volatile memory (NVM) is restored).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Padgaonkar et al. US Patent 5,014,191.

In regards to claim 6, Padgaonkar does not disclose said read protection flag is stored within said non-volatile memory unit, however the protection keys are made of the same non-volatile memory (NVM) as the memory unit (due to limitations in manufacturing since fabrication lines are custom tailored to produce high yield in a specific class of chips (FLASH, CMOS Sensor, FRAM, etc)) and Padgaonkar discloses the protection keys are located on the same chip as the NVM unit. Therefore it would have been obvious to place the protection flags within the NVM unit for the purpose of reducing signal path length of the protection flags to the High Voltage Generator (figure 1 element 114) needed to program said protection flags, good design practice minimizes signal path length to reduce attenuation and interference.

In regards to claim 14, Padgaonkar discloses a single integrated circuit microcontroller comprising:

an erasable/programmable non-volatile memory unit including a first portion adapted to store certain firmware in figure 2 element 108;

a read protection flag in figure 2 element 202; and

a logic portion which is adapted to detect when a special mode is activated, to check said read protection flag upon detecting a special mode, and to allow external

access to said first portion of said non-volatile memory unit only if said special mode is activated and said read protection flag is cleared in figure 2 element 200 and column 1 line 66 through column 2 line 5.

Padgaonkar does not disclose said read protection flag is stored within said non-volatile memory unit, however the protection keys are made of the same non-volatile memory (NVM) as the memory unit (due to limitations in manufacturing since fabrication lines are custom tailored to produce high yield in a specific class of chips (FLASH, CMOS Sensor, FRAM, etc)) and Padgaonkar discloses the protection keys are located on the same chip as the NVM unit. Therefore it would have been obvious to place the protection flags within the NVM unit for the purpose of reducing signal path length of the protection flags to the High Voltage Generator (figure 1 element 114) needed to program said protection flags, good design practice minimizes signal path length to reduce attenuation and interference.

Claims 8-13 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Padgaonkar et al. US Patent 5,014,191 in view of Sibigtroth et al. US Patent 5,251,304.

In regards to claim 8, Padgaonkar discloses the microcontroller of claim 1 further comprising:

at least one input/output pin, and wherein said logic portion comprises:

control logic which is adapted to detect when said special mode is activated in figure 3 MC/MP input, to check said read protection flag upon detecting a special mode in figure 3 SO input, and to erase said non-volatile memory unit and clear said read protection flag if said read protection flag is set and said special mode is activated in column 2 lines 15-22 and 40-44.

However, Padgaonkar does not disclose a switching logic which is adapted to selectively connect and disconnect said at least one input/output pin to and from said non-volatile memory unit; and the control logic is communicatively coupled to said switching logic and said control logic being further adapted to selectively communicate signals to said switching logic, effective to connect said at least one input/output pin to said non-volatile memory only if said special mode is activated and said read protection flag is cleared.

Sibigtroth discloses a means of preventing external access to internally stored data and program code by using isolation buffers (figure 2 elements 58 and 60) to selectively connect the internal data bus (figure 1 element 24) to the external data bus (figure 1 element 30) by way of processor state information (Instruction Fetch, Data Read, Data Write) and a programmable security device (figure 1 element 20). Padgaonkar discloses prevention of accessing data contents within the on-board NVM, but does not provide an explicit method of doing so (other that providing the READ, WRITE, INT, EXT signals). The inhibition of the reading of the on-board NVM by an external entity can be accomplished via one of two methods; inhibiting the input to the

NVM, or inhibiting the output of the NVM. Sibigtroth discloses a means for doing the latter.

Therefore it would have been obvious at the time of invention to one of ordinary skill in the art to incorporate Sibigtroth's bus isolation mechanism within Padgaonkar (minor modification to the selection signals of multiplexor 126 of figure 1 would produce Sibigtroth's bus isolation mechanism). Padgaonkar's and Sibigtroth's inventions can be combined in a straightforward manner by connecting the READ and WRITE outputs of Padgaonkar's figure 3 with Sibigtroth's DATA READ and DATA WRITE of figure 2, connecting the TR signal of Padgaonkar's figure 3 with Sibigthroth's INSTRUCTION FETCH of figure 2 and the SO signal of Padgaonkar's figure 3 with Sibigthroth's ENABLE of figure 2. Given this arrangement, Sibigtroth's isolation buffer state would be dependent upon the special mode of Padgaonkar. Likewise, since Sibigtroth is clearly interested in the processor state information to determine the state of the isolation buffers, it would have been obvious at the time of invention to one of ordinary skill in the art to have Sibigtroth's isolation buffers' state to be dependent upon Padgaonkar's special mode.

In regards to claim 9, Sibigtroth discloses in figure 1 the microcontroller further comprising a micro-control unit (element 14) which is selectively connected to said input/output pins (element 30 interface with element 12) and to said non-volatile memory unit (element 13) by use of said switching logic (element 18).

In regards to claim 10, Padgaonkar discloses the microcontroller further comprising a random access memory unit which is communicatively coupled to said micro-control unit in column 1 lines 15-20.

In regards to claim 11, Padgaonkar discloses the microcontroller further comprising a read-only memory unit which is communicatively coupled to said micro-control unit in column 1 lines 15-20.

In regards to claim 12, Padgaonkar discloses said micro-control unit comprises a microprocessor in figure 1 element 14.

In regards to claim 13, Padgaonkar discloses said control logic is communicatively coupled to said at least one input/output pin and is adapted to detect a special mode upon sensing a predetermined sequence of signals communicated to said at least one input/output pin in column 1 line 65 through column 2 line 5.

In regards to claim 23, Padgaonkar does not explicitly disclose said step of allowing external access to said first portion of said memory unit comprises electrically connecting said memory unit to a plurality of input/output pins.

Sibigtroth discloses a means of preventing external access to internally stored data and program code by using isolation buffers (figure 2 elements 58 and 60) to selectively connect the internal data bus (figure 1 element 24) to the external data bus

(figure 1 element 30) by way of processor state information (Instruction Fetch, Data Read, Data Write) and a programmable security device (figure 1 element 20). Padgaonkar discloses prevention of accessing data contents within the on-board NVM, but does not provide an explicit method of doing so (other that providing the READ, WRITE, INT, EXT signals). The inhibition of the reading of the on-board NVM by an external entity can be accomplished via one of two methods; inhibiting the input to the NVM, or inhibiting the output of the NVM. Sibigtroth discloses a means for doing the latter.

Therefore it would have been obvious at the time of invention to one of ordinary skill in the art to incorporate Sibigtroth's bus isolation mechanism within Padgaonkar (minor modification to the selection signals of multiplexor 126 of figure 1 would produce Sibigtroth's bus isolation mechanism). Padgaonkar's and Sibigtroth's inventions can be combined in a straightforward manner by connecting the READ and WRITE outputs of Padgaonkar's figure 3 with Sibigtroth's DATA READ and DATA WRITE of figure 2, connecting the TR signal of Padgaonkar's figure 3 with Sibigthroth's INSTRUCTION FETCH of figure 2 and the SO signal of Padgaonkar's figure 3 with Sibigthroth's ENABLE of figure 2. Given this arrangement, Sibigtroth's isolation buffer state would be dependent upon the special mode of Padgaonkar. Likewise, since Sibigtroth is clearly interested in the processor state information to determine the state of the isolation buffers, it would have been obvious at the time of invention to one of ordinary skill in the art to have Sibigtroth's isolation buffers' state to be dependent upon Padgaonkar's special mode.

In regards to claim 24, Sibigtroth discloses said step of electrically connecting said memory unit to a plurality of input/output pins is performed by use of at least one switching circuit in figure 2 elements 58 and 60.

In regards to claim 25, Padgaonkar discloses 25) The method of claim 24 wherein said special mode is detected by sensing a predetermined sequence of signals on said plurality of input/output pins in column 2 lines 2-4.

Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Padgaonkar et al. US Patent 5,014,191 in view of Lee et al. US Patent 5,930,826.

In regards to claim 15, Padgaonkar does not disclose said memory unit further comprises a second portion and wherein said logic portion is adapted to allow external access to said second portion of said non-volatile memory unit during said special mode when said read protection flag is set and when said read protection flag is cleared.

Lee discloses protection of a flash memory in which portions of the memory may be protected from being read by an external source while other portions of the memory are unprotected via RD-bit in figure 1 element 83. Lee recognizes the need for protection of the contents of a flash memory in column 1 lines 23-29, and that flexibility in protecting only portions of the flash memory is desirable in column 2 lines 33-48. Therefore it would have been obvious to one of ordinary skill in the art at the time of

invention to have multiple sections of the flash memory wherein each has its own level of protection.

In regards to claim 16, Padgaonkar discloses said logic portion is further adapted to detect an external request to access said first portion of said memory unit when said special mode is activated, to erase said certain firmware in response to said external request if said read protection flag is set, and to allow external access to said first portion of said memory unit only after said certain firmware is erased in column 2 lines 15-22.

In regards to claim 17, Padgaonkar discloses said logic portion is adapted to detect a request to access said first portion of said memory unit when said special mode is activated, to program over said certain firmware in response to said request if said read protection flag is set, and to allow external access to said first portion of said memory unit only after said programming is complete in column 2 lines 15-22.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Padgaonkar et al. US Patent 5,014,191 in view of Sibigtroth et al. US Patent 5,251,304 as applied to claims 8-13 and 23-25 above, and further in view of Lee et al. US Patent 5,930,826.

In regards to claim 26, neither Padgaonkar nor Sibigtroth said memory unit further comprises a second portion, said method further comprising the steps of:

detecting a request to access said second portion of said memory unit while said special mode is activated; and

allowing access to said second portion of said memory unit in response to said request when said read protection flag is set and when said read protection flag is cleared.

Lee discloses protection of a flash memory in which portions of the memory may be protected from being read by an external source while other portions of the memory are unprotected via RD-bit in figure 1 element 83. Lee recognizes the need for protection of the contents of a flash memory in column 1 lines 23-29, and that flexibility in protecting only portions of the flash memory is desirable in column 2 lines 33-48. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have multiple sections of the flash memory wherein each has its own level of protection.

Allowable Subject Matter

Claims 18 and 19 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

In regards to claim 18 none of the prior art of record discloses a flash memory control circuit communicating a third signal to said special mode detection circuit when said read protection flag is cleared and said special mode is activated, wherein said

third signal is effective to cause said special mode detection circuit to generate said second signal only after receipt of said third signal. This "feedback signal" from the flash memory control circuit to the mode detection circuit is not disclosed in any of the prior art of record. For this reason, claim 18 is found allowable over the prior art of record.

Claim 19 is allowable as dependent upon allowed claim 18.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (703)305-3304. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703)306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PB

Mano Padmanabhan 7/26/04

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER